Barrier Coatings and Stability of Thin Film Solar Cells

3rd Quarterly Report - Phase I:

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Subcontractor: **Pacific Northwest National Laboratory**

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1. OBJECTIVES/APPROACH

The key objectives of this program are to develop low cost barrier coatings for CdTe and CIS solar cells and to develop an improved understanding of mechanisms affecting the stability of CdTe solar cells. The scope of this work entails investigation of multilayer, barrier coatings for solar cells and studies of stability issues for CdTe solar cells. The work is structured into three main tasks: (1) Barrier layer coatings for CdTe and CIS solar cells; (2) Modeling of mechanisms influencing CdTe stability; (3) Experimental studies of CdTe cells supporting Tasks 1 and 2.

2. PROGRESS THIS REPORTING PERIOD

Efforts concentrated on working with SSI to initiate accelerated testing of SSI circuits with and without barrier layer coatings. Details of the approach and some early results are discussed below.

2.1 Accelerated Lifetests

Six SSI circuits have now undergone one thousand hours of accelerated lifetesting. Specifically, these circuits were subjected to an environment of 60ºC and 90% relative humidity for 1000 hours. Current voltage measurements were taken periodically by removing the circuits from the chamber, carrying out the measurement, and then replacing the circuits in the chamber. The approach used in applying barrier coatings to the SSI circuits was discussed in our last quarterly. Features of the multilayer coatings are given Table 1, and data for estimated cell efficiency versus time of exposure to 60/90 conditions are given for these circuits in Figures 1,2,3,4 and 5. In general, circuits with a relatively thick first polymer layer have exhibited good performance. Circuit # 4 essentially shows no degradation after the accelerated test. Circuits #7 and #9 were cleaned in a similar manner to #4 and coated with the initial 3.5 μm polymer layer, but show 5% to 10% degradation. It may be that a slightly thicker first layer was needed in order to achieve the performance of #4. It is clear, however, that we are close to defining a process that will allow circuits to survive 1000 hours at 60/90.

2.2 Characterization of Circuit Surfaces

Surfaces of as-received material and SSI circuits with initial layers of 0.5 μm have been examined. Figures 6 through 9 give results of these studies. Characterization of circuits with initial polymer thicknesses of 3.5 μm will be carried out during the next quarter. A nodule on an as-received circuit surface is shown in Figure 6. The image shows the ZnO on the outer surface of the nodule. Analysis of the interior of the nodule clearly established that the nodule is not simply ZnO, but contains Cu, In, Se and sulfur. Thus the nodule existed prior to ZnO deposition. An image of a coated smooth surface area is shown in Figure 7. As noted above, the initial polymer layer is approximately 0.5 μm. If the complete device surface were as smooth as the area shown in Figure 7, one would expect an initial layer of 0.5 μm to be adequate for protecting SSI circuits from moisture

ingress. Examination of coated surfaces in the vicinity of nodules indicates the need for thicker planarizing layers.

Two coated nodules are shown in Figures 8 and 9. The nodule shown in Figure 8 is 5 to 7 μm in height. Even though the initial layer is only 0.5 μm thick, this coating appears adequate for preventing moisture ingress. The case described by Figure 9 is different, however. The nodule is greater than 10 μm, and the top of the nodule appears to be exposed. This image illustrates the need for a thicker initial layer for the SSI circuits. The image also illustrates how moisture usually penetrates film structures, namely, through an opening created by a protruding defect.

Table 1 - Characteristics Of Barrier Coatings

Cell # 3	No Barrier Coating
Circuit # 12	First Polymer Layer of 0.5 μm, and mild cleaning
Circuit # 5	First Polymer layer of 3.5 μm, and cleaning
Circuit # 4, 7 and 9	First Polymer layer of 3.5 μm, and vigorous cleaning

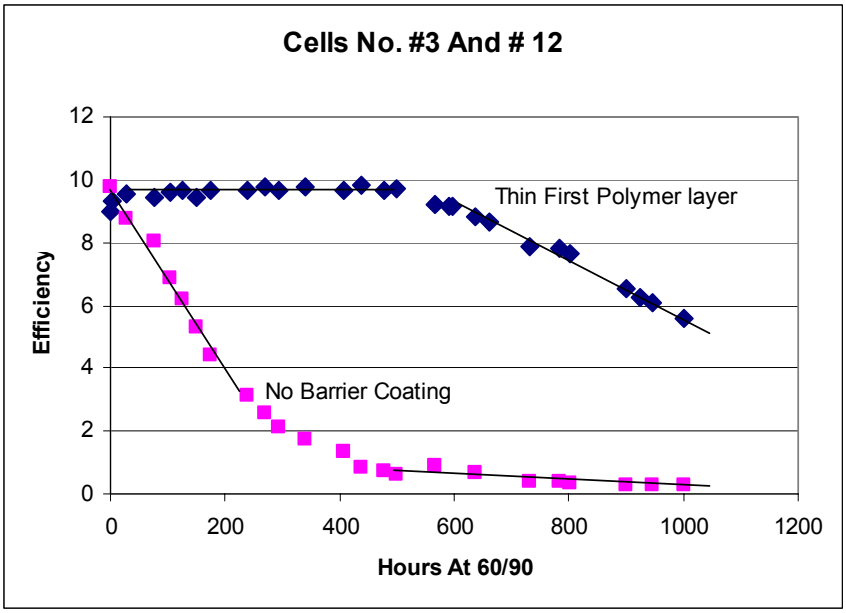

Figure 1. Lifetests for an uncoated SSI circuit (No. 3) and a coated circuit (No. 12) for which the first polymer layer is 0.5 µm.

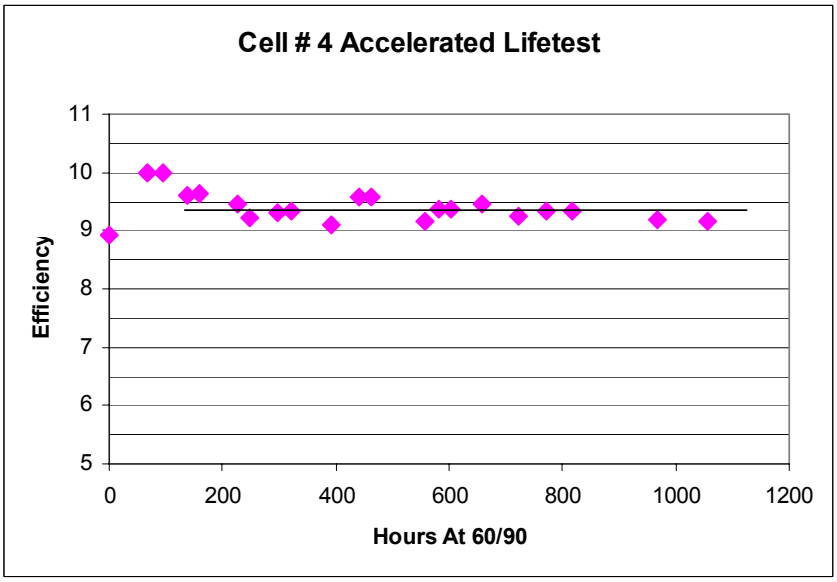

Figure 2. Results for a circuit which received vigorous cleaning and a multilayer coating with the first polymer layer being 3.5 µm.

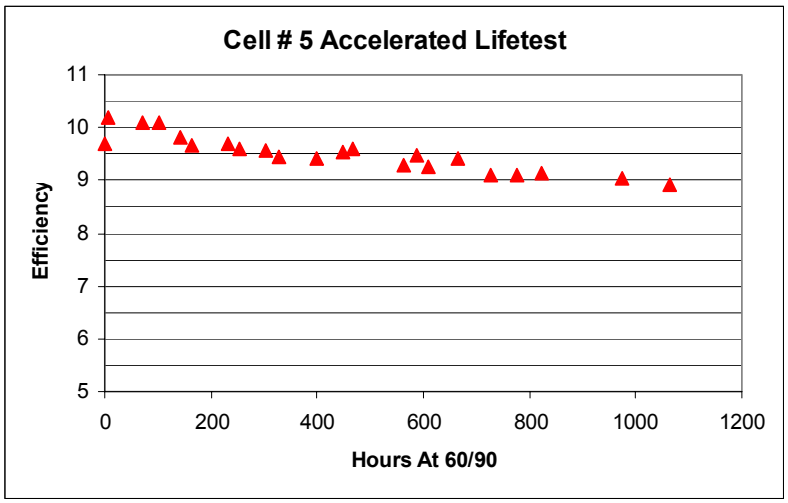

Figure 3. Results for a circuit which received mild cleaning and a multilayer coating with the first polymer layer being 3.5 µm

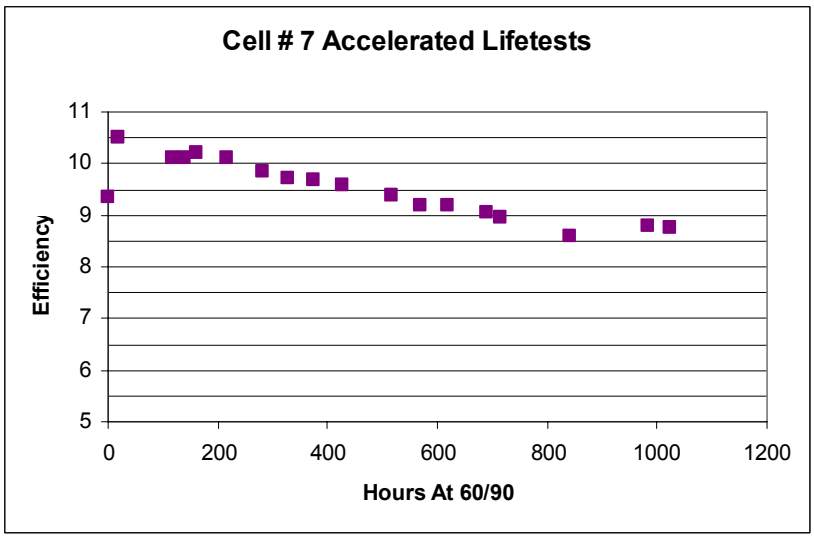

Figure 4. Results for a circuit which received vigorous cleaning and a multilayer coating with the first polymer layer being 3.5 µm

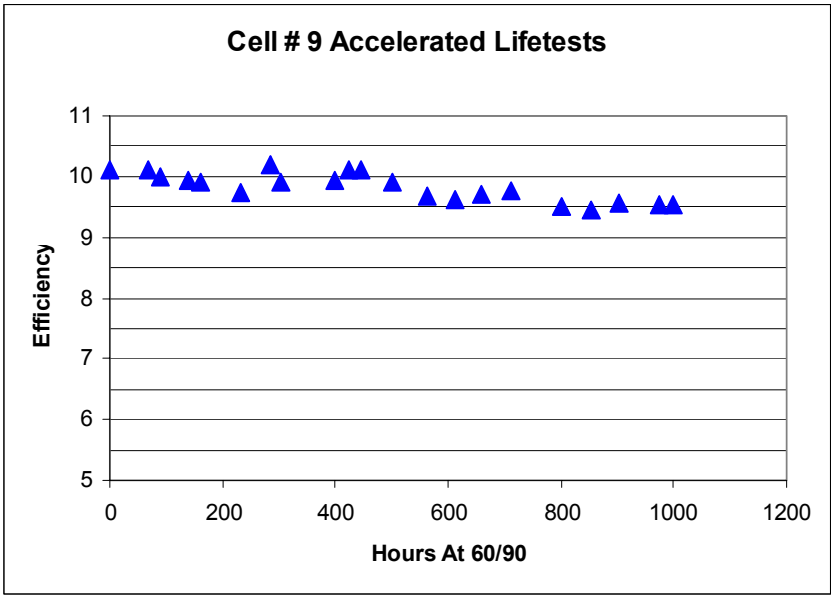

Figure 5. Results for a circuit which received vigorous cleaning and a multilayer coating with the first polymer layer being 3.5 μm

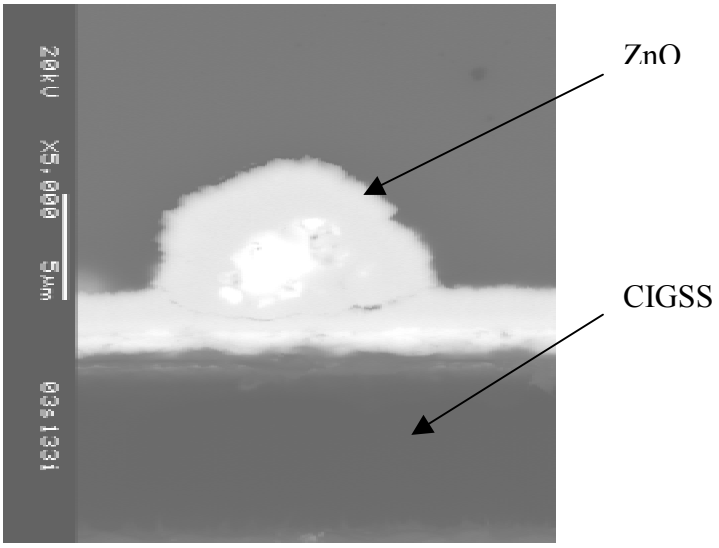

Figure 6. Electron micrograph showing nodule in as-received film surface.

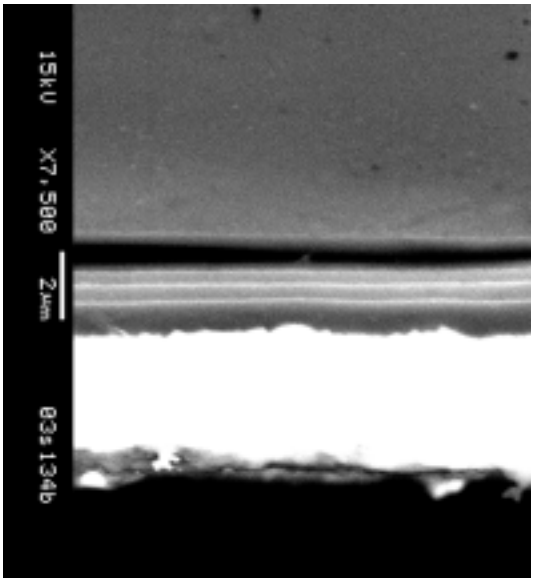

Figure 7. Barrier coating in area of smooth surface. Initial polymer layer was 0.5 μm.

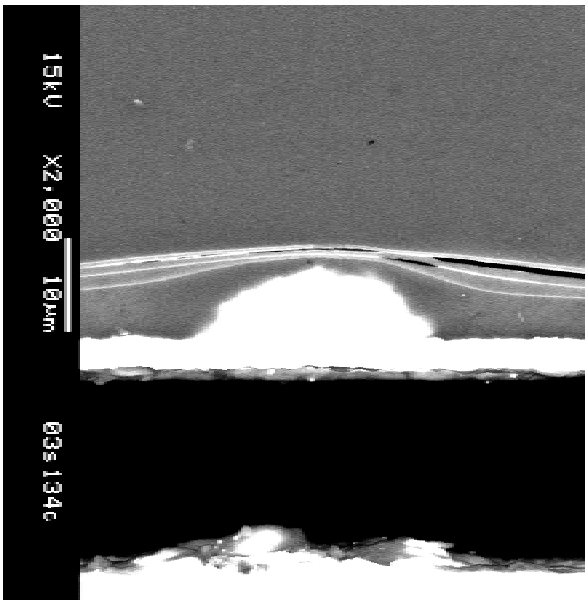

Figure 8. Coating over 5 μm nodule. Initial polymer layer was 0.5 μm.

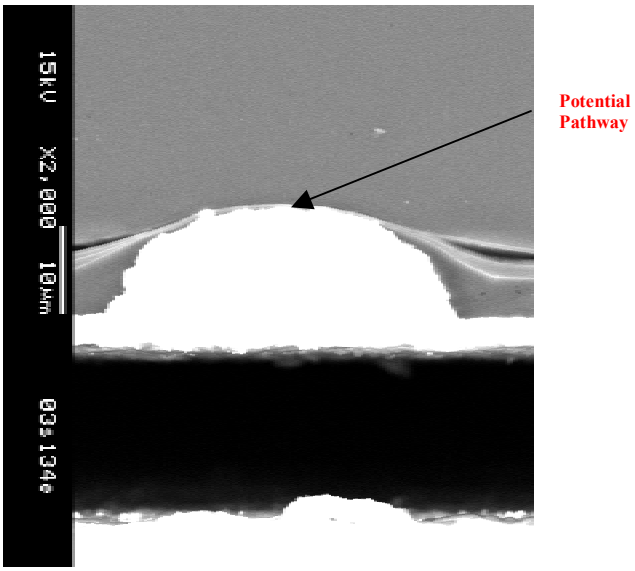

Figure 9. Coating over 12 μm nodule. Initial polymer layer was 0.5 μm.